REMARKS

Claims 1-20 remain pending. Claims 1, 3, 10, and 17 have been amended. No new matter has been added as a result of these amendments.

Claim Rejections – 35 U.S.C. §112

Claim 3 is rejected under 35 U.S.C. 112, first paragraph, as allegedly failing to comply with the written description requirement. Specifically, the rejection stated the original specification allegedly failed to teach components of said first circuit are placed in a fixed state during manufacturing.

As amended, Claim 3 recites in part, "said plurality of individually-configured components of said first circuit are placed in a fixed state during a configuration of said timer circuit before operation of said timer circuit," which is supported, for example, by Figure 3 and Page 10, lines 7-17. Accordingly, Applicants respectfully submit that Claim 3 complies with 35 U.S.C. 112, first paragraph.

Claim Rejections – 35 U.S.C. §103

Claims 1-20 are rejected under 35 U.S.C. 103(a) as being allegedly unpatentable over Hara et al (US 5,994,937), hereinafter "Hara," in view of Kwon (US 5,926,045), hereinafter "Kwon," further in view of Mitsuishi (US 6,031,366), hereinafter "Mitsuishi," and yet further in view of Saeki (US 6,388,490), hereinafter "Saeki."

Applicants respectfully point out that the Examiner has the burden of establishing a prima case of obviousness. To establish a prima facie case of obviousness, three basic

criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim features. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on Applicant's disclosure. In re Vaeck, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991). See MPEP 2100-126. Specifically, "all words in a claim must be considered when judging the patentability of that claim against the prior art." *In re Wilson*, 424 F.2d., 1382 (CCPA 1970).

Moreover, in response to the recent U.S. Supreme Court decision in *KSR Int'l Co. v. Teleflex, Inc.* (U.S. 2007), new guidelines were set forth for examining obviousness under 35 U.S.C. 103. The U.S. Supreme Court reaffirmed the *Graham* factors and, while not totally rejecting the "teachings, suggestion, or motivation" test, the Court appears to now require higher scrutiny on the part of the U.S. Patent & Trademark Office. In accordance with the recently submitted guidelines, it is "now necessary to identify the reason" why a person of ordinary skill in the art would have combined the elements of cited references, or at least describe the pertinence of the elements set forth in the cited disclosure, in the manner presently claimed.

Applicants contend that the cited references fail to teach or suggest all the claimed elements.

Claim 1:

Claim 1 recites in part:

> an output stage coupled to a configurable delay element, wherein said configurable delay element comprises a plurality of selectively-activated components operable to adjust a delay through said timer circuit; and a pull-down path coupled to said output stage and comprising a first circuit configured to provide a selectable amount of pull down current, for varying said delay through said timer circuit, wherein said first circuit comprises a plurality of individually-configured components, wherein said plurality of selectively-activated components are of a different component type than said plurality of individually-configured components, said pull-down path further comprising a second circuit for varying said delay through said timer circuit based upon temperature, wherein said second circuit is operable to vary said delay based upon a reference signal, wherein said reference signal varies said pull-down current, and wherein said delay is inversely proportional to said temperature (emphasis added).

The Examiner looks to Hara to teach "adjust[ing] a delay through said timer circuit." However, Hara simply does not teach or suggest "adjust[ing] a delay through said timer circuit," as claimed in Claim 1.

Further, rather than teaching or suggesting "varying said delay through said timer circuit based upon temperature…wherein said delay is inversely proportional to said temperature," as claimed in Claim 1, Hara teaches away from claimed embodiments by teaching a delay element that provides consistent delay by compensating for process and power supply voltage variations that would normally change the delay (Column 3, lines 11-14, and 50-53). As discussed below, neither Kwon nor Mitsuishi nor Saeki remedy this deficiency.

The rejection contends that the combination of Kwon and Mitsuishi with Hara teach a pull-down path that is a variable current source, as claimed in Claim 1. Applicants respectfully disagree. Neither Hara nor Kwon nor Mitsuishi teaches or suggests a pull-down path providing a selectable amount of pull down current, as claimed in Claim 1.

Further, Hara teaches away from Kwon and Mitsuishi, whether the cited references are considered together or separately. The rejection notes that Hara teaches a fixed current source. The combination of Kwon and Mitsuishi teach away from Hara's fixed current source, as both teach a variable current source. Further, neither Kwon nor Mitsuishi teach or suggest varying the delay of a timer circuit based upon temperature, as claimed in Claim 1. Therefore, there is no motivation to combine Kwon and Mitsuishi with Hara. Assuming, *arguendo,* Hara combined with Kwon and Mitsuishi, collectively they fail to teach or suggest, "varying said delay through said timer circuit based upon temperature…wherein said delay is inversely proportional to said temperature," as claimed in Claim 1.

Applicants respectfully submit that Hara, Kwon, Mitsuishi and/or Saeki do not teach or suggest "adjust[ing] a delay through said timer circuit; and…a selectable amount of pull down current, wherein said first circuit comprises a plurality of individually-configured components… varying said delay through said timer circuit based upon temperature…wherein said delay is inversely proportional to said temperature," as claimed in Claim 1. For this reason, Applicants respectfully submit that Claim 1 is in

condition for allowance. Further, Applicants respectfully assert that dependent Claims 2-9 are patentable by virtue of their dependency, as well as for the additional patentable features they recite.

Claim 10:

Claim 10 recites in part:

> a plurality of selectively-activated components operable to adjust a delay through said timer circuit; and a pull-down path coupled to said output stage and comprising a first circuit configured to provide a selectable amount of pull down current for varying said delay through said timer circuit, wherein said first circuit comprises a plurality of individually-configured components, wherein said plurality of selectively-activated components are of a different component type than said plurality of individually-configured components, said pull-down path further comprising a second circuit for varying said delay through said timer circuit based upon temperature, wherein said second circuit is operable to vary said delay based upon a reference signal, wherein said reference signal varies said pull-down current, wherein said delay is inversely proportional to said temperature, and wherein said reference signal is derived from a band gap reference circuit (emphasis added).

Independent Claim 10 is patentable for at least the same or similar reasons as recited above. Applicants respectfully submit that Hara, Kwon, Mitsuishi and/or Saeki do not teach or suggest "adjust[ing] a delay through said timer circuit; and…a first circuit configured to provide a selectable amount of pull down current, wherein said first circuit comprises a plurality of individually-configured components…varying said delay through said timer circuit based upon temperature…wherein said delay is inversely proportional to said temperature," as claimed in Claim 10. Accordingly, Applicants respectfully submit that Hara, Kwon, Mitsuishi and/or Saeki do not teach all of the claimed features of Claim 10, and for this reason, Applicants respectfully submit that Claim 10 is in

condition for allowance. Further, Applicants respectfully assert that dependent claims 11-16 are patentable by virtue of their dependency, as well as for their additional patentable features.

Claim 17:

Claim 17 recites in part:

> during configuration of said timer circuit, setting a first plurality of configuration bits which control the amount of elements coupled to an output stage of said timer circuit to set an amount of delay through said timer circuit; during said configuration, setting a second plurality of configuration bits which control an amount of pull down current through a pull down path of said timer circuit to set an amount of delay through said timer circuit, said pull down path coupled to said output stage, wherein said pull down path comprises a plurality of individually-configured components, and wherein each of said plurality of individually-configured components corresponds to a respective configuration bit of said plurality of configuration bits; and during operation of said timer circuit, varying said delay of said timer circuit in response to a varying of a reference signal, wherein said reference signal varies said pull-down current, wherein said delay of said timer circuit is inversely proportional to a temperature of said timer circuit (emphasis added).

Independent Claim 17 is patentable for at least the same or similar reasons as recited above. Applicants respectfully submit that Hara, Kwon, Mitsuishi and/or Saeki do not teach or suggest "set[ting] an amount of delay through said timer circuit; during said configuration, setting a second plurality of configuration bits which control an amount of pull down current through a pull down path of said timer circuit to set an amount of delay through said time circuit,...wherein said pull down path comprises a plurality of individually-configured components...wherein said delay of said timer circuit is inversely proportional to a temperature of said timer circuit," as claimed in Claim 17. Accordingly, Applicants respectfully submit that Hara, Kwon, Mitsuishi and/or Saeki do

not teach all of the claimed features of Claim 17, and for this reason, Applicants respectfully submit that Claim 17 is in condition for allowance. Further, Applicants respectfully assert that dependent Claims 18-20 are patentable by virtue of their dependency.

For the above reasons, Applicants request reconsideration and withdrawal of the rejections under 35 U.S.C. §103.

CONCLUSION

In light of the above listed remarks, reconsideration of the rejected Claims 1-20, is requested. Based on the arguments presented above, it is respectfully submitted that Claims 1-20 overcome the rejections of record and, therefore, allowance of Claims 1-20 is earnestly solicited.

Please charge any additional fees or apply any credits to our PTO deposit account number: 50-4160.

Respectfully submitted,

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